A Permanent Magnet Brushless DC Motor Drive Based Voltage Controlled Power Factor Correction SEPIC Converter

Abstract-This paper deals with a SEPIC DC–DC converter as a power-factor-correction converter for a permanent magnet (PM) brushless dc motor (PMBLDCM).It is fed through a diode bridge r fier from a single-phase ac mains. A three-phase voltage-source inverter is used as an electronic commutator to operate the PMBLDCM. A speed control scheme for voltage source inverter (based PMBLDCM is developed and it is based on the control of the dc link voltage reference as an equivalent to the reference speed. The stator currents of the PMBLDCM during step change in reference speed are controlled within the specified limits by an addition of a rate limiter in the reference dc link voltage. The proposed PMBLDCM drive (PMBLDCMD) is designed and modeled, its performance is evaluated in MATLAB–SIMULINK environment. Simulated results are presented to demonstrate an improved power factor at ac mains of the PMBLDCMD system.

BALAHEMALATHA.R,SARMILA HAR BEAGAM.K,SRINIVAS.K.N

1.INTRODUCTION

The Brushless DC (BLDC) motor is the ideal choice for applications that require high reliability, high efficiency, and high power-to-volume ratio. It is considered to be a high performance motor that is capable of providing large amounts of torque over a vast speed range. BLDC motors do not have brushes and must be electronically commutated. Thus they have higher efficiency, long operating life, rugged construction and noiseless operation. BLDC motor implements the basic principle of conventional DC motors except that the stator has three phase windings whereas the rotor has pole magnets. The hall sensors are embedded in the motor and it detects the rotor position. The decoder decodes the position of the rotor and produces gate pulses to trigger the six-switch inverter to produce AC voltage that energizes the stator windings to produce current. Recent developments in power electronics, microelectronics and modern control technologies have greatly influenced the wide spread use of permanent magnet motors.

A PMBLDCM has the developed torque proportional to its phase current and its back electromotive force (EMF), which is proportional to the speed. Under variable speed operation, a constant current in the stator windings with variable voltage across its terminals maintains constant torque in a PMBLDCM. A speed control scheme is proposed and it uses a reference voltage at dc link proportional to the desired speed of the permanent-magnet brushless direct current (PMBLDC) motor [1].

The PMBLDC drive consists of a VSI and the PMBLDC motor and it is usually powered through a diode bridge rectifier fed from a single phase AC mains followed by a DC link capacitor. This arrangement suffers from power quality disturbances at the ac mains in terms of poor power factor (PF) of the order of 0.728 [1]. Power factor correction method is a publications regarding PFC in PMBLDCMDs despite many PFC topologies for switched mode power supply and battery charging applications. This paper deals with an application of a PFC converter for the speed control of a PMBLDCMD.A SEPIC dc–dc converter is used as a PFC converter because of its continuous input and output currents, small output filter, and wide output voltage range as compared to other single switch converters [3].

2.PROPOSED SPEED CONTROL SCHEME OF PMBLDC MOTOR

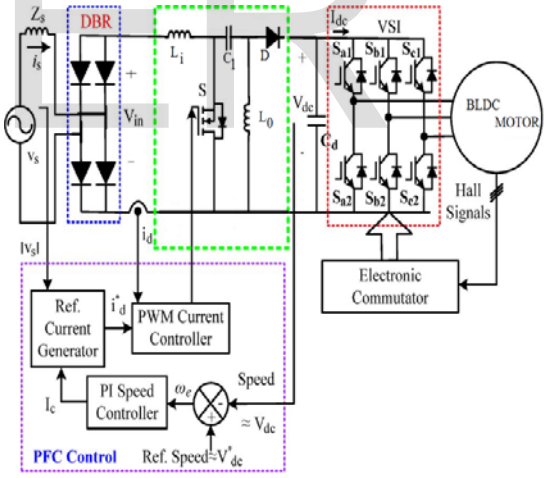


Fig. 1. Control scheme of the proposed SEPIC PFC converter-fed VSI-based PMBLDCMD.

Fig 1 shows the speed control scheme which is based on the control of the dc link voltage reference as an equivalent to the reference speed. The rotor position signals acquired by Hall-effect sensors are used by an electronic commutator to

generate switching sequence for the VSI and it is required only at the commutation points [1]-[3].

The SEPIC DC–DC converter controls the dc link voltage using capacitive energy transfer and is based on the current balance of the capacitor. This results in non pulsating input and output currents [4]. The proposed PFC converter is operated at a high switching frequency for fast and effective control and also has an advantage of a small size filter. A metal–oxide–semiconductor field-effect transistor (MOSFET) is used in the proposed PFC converter for high frequency operation, whereas insulated gate bipolar transistors (IGBTs) are used in the VSI Bridge feeding the PMBLDCM because of its operation at lower frequency compared to the PFC converter. For continuous-conduction-mode operation of the converter, the PFC control scheme uses a current multiplier approach with a current control loop inside the speed control loop.

The control loop begins with the processing of voltage error (V_e) obtained after the comparison of sensed dc link voltage (V_{dc}) and a voltage (V^*_{dc}) equivalent to the reference speed, through a proportional–integral (PI) controller to give the modulating control signal (I_c). This signal (I_c) is multiplied with a unit template of input ac voltage to get the reference dc current (I^*_d) and compared with the dc current (I_d) sensed after the DBR. The resultant current error (I_e) is amplified and compared with a sawtooth carrier wave of fixed frequency (f_s) to generate the pulse width modulation (PWM) pulse for the SEPIC converter. Its duty ratio (D) at a switching frequency (f_s) controls the dc link voltage at the desired value. For the control of current to PMBLDCM through VSI during the step change of the reference voltage due to the change in the reference speed, a rate limiter is introduced, which limits the stator current of the PMBLDCM within the specified value which is considered as double the rated current[1].

III. DESIGN OF PFC SEPIC CONVERTER-BASED PMBLDCMD

The proposed PFC SEPIC converter is designed for a PMBLDC motor drive with main considerations on the speed control and power factor improvement on the AC mains. The dc link voltage of the PFC converter is given as

$$V_{dc}=V_{in}D/(1-D) \quad (1)$$

where V_{in} is the average output of the DBR for a given ac input voltage (V_s) related as

$$V_{in}=2\sqrt{2}V_s/\pi \quad (2)$$

The SEPIC converter uses a boost inductor (L_i) and a capacitor (C_1) for energy transfer. Their values are given as

$$L_i=DV_{in}/\{f_s(\Delta I_{Li})\} \quad (3)$$

$$C_1=DI_{dc}/\{f_s(\Delta V_{c1})\} \quad (4)$$

where ΔI_{Li} is a specified inductor current ripple, ΔV_{c1} is a specified voltage ripple in the intermediate capacitor (C_1), and I_{dc} is the current drawn by the PMBLDCM from the dc link.

A ripple filter is designed for ripple-free voltage at the dc link of the SEPIC converter. The inductance (L_o) of the ripple filter restricts the inductor peak-to-peak ripple current (ΔI_{L0}) within a specified value for the given switching frequency (f_s), whereas the capacitance (C_d) is calculated for the allowed ripple in the dc link voltage (ΔV_{Cd}) [5],[6]. The values of the ripple filter inductor and capacitor are given as

$$L_0 = (1-D)V_{dc} / f_s\Delta I_{L0} \quad (5)$$

$$C_d = I_{dc} /(2\omega\Delta V_{Cd}) \quad (6)$$

The PFC converter is designed for a base dc link voltage of V_{dc} = 360 V at V_s = 220 V for f_s = 40 kHz,I_s= 4.52 A, ΔI_{Li} = 0.452 A (10% of I_{dc}), I_{dc} = 3.21 A, ΔI_{L0} = 3.21 A (≈I_{dc}) and ΔV_{c1} = 220 V (≈V_s).

The design values are obtained as L_i = 5.90 mH, C_1 = 0.2910 μF, L_o = 0.676 mH, and C_d = 2545 μF.

IV. MODELING OF PFC CONVERTER-BASED PMBLDCMD

The PFC converter and PMBLDCMD are the main components of the proposed drive, which are modeled by mathematical equations, and a combination of these models represents the complete model of the drive.

A. PFC Converter

The modeling of the PFC converter consists of the modeling of a speed controller, a reference current generator, and a PWM controller as given hereinafter.

1)Speed Controller: The speed controller is a PI controller which closely monitors the speed error as an equivalent voltage error and generates the control signal(I_C) to minimize the error. If at the k^{th} instant of time, $V^*_{dc}(k)$ is the reference dc link voltage and $V_{dc}(k)$ is the voltage sensed at the dc link, then the voltage error $V_e(k)$ is given as

$$V_e(k)=V^*_{dc}(k) - V_{dc}(k) \quad (7)$$

The PI controller output $I_c(k)$ at the k^{th} instant after processing the voltage error $V_e(k)$ is given as

$$I_c(k)=I_c(k-1)+ k_p\{V_e(k)-V_e(k-1)\}+ k_i V_e(k) \quad (8)$$

where k_p and k_i are the proportional and integral gains of the PI controller.

(2)Reference Current Generator: The reference current at the input of the SEPIC converter (i^*_d) is

$$i_d^*=I_c(k).uv_s \quad (9)$$

where,

uv_s is the unit template of the ac mains voltage, calculated as

$$uv_s = v_d/V_{sm} \; ; \quad v_d=|v_s| \; ; \quad v_s = V_{sm}\sin \omega t \quad (10)$$

where,

V_{sm} is the amplitude (in volts)

ω is the frequency (in radians per second) of the ac mains voltage.

(3)PWM Controller: The reference input current of the SEPIC converter(i^*_d) is compared with its current (i_d) sensed after DBR to generate the current error $\Delta i_d= (i^*_d- i_d)$.This current error is amplified by gain k_d and compared with fixed frequency (f_s) carrier waveform $m_d(t)$ [5] to get the switching signal for the IGBT of the PFC SEPIC converter as

$$\text{if} \quad k_d \Delta i_d > m_d(t) \quad \text{then S=1} \quad (11)$$

$$\text{if} \quad k_d \Delta i_d < m_d(t) \quad \text{then S=0} \quad (12)$$

where S denotes the switching of the IGBT of the SEPIC converter and its value "1" and "0" represent "ON" and "OFF" respectively.

B. PMBLDCMD

The PMBLDCMD consists of an electronic commutator,a VSI, and a PMBLDCM.

(1)Electronic Commutator: The rotor position signals acquired by the Hall-effect position sensors and are used by the electronic commutator to generate the switching sequence for the VSI as shown in Table I [2],[6].

TABLE I
ELECTRONIC COMMUTATOR OUTPUT BASED ON THE HALL-EFFECT SENSOR SIGNALS

HALL SIGNALS			SWITCHING SIGNALS					
Ha	Hb	Hc	Sa1	Sa2	Sb1	Sb2	Sc1	Sc2
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	1	0
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
1	0	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0	0
1	1	0	0	0	1	0	0	1
1	1	1	0	0	0	0	0	0

(2) Voltage Source Inverter: The output of VSI to be fed to phase "a" of the PMBLDC motor is calculated from the equivalent circuit of a VSI-fed PMBLDCM shown in Fig. 2 as

$$v_{ao} =(V_{dc} / 2) \quad \text{for } Sa1 = 1 \quad (13)$$

$$v_{ao} =(- V_{dc}/ 2) \quad \text{for } Sa2 = 1 \quad (14)$$

$$v_{ao} =0 \quad \text{for } Sa1 = 0, \text{ and } Sa2 = 0 \quad (15)$$

$$v_{ao} = v_{ao} - v_{no} \quad (16)$$

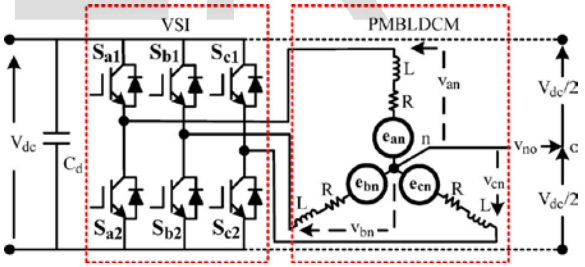


Fig. 2 Equivalent circuit of a VSI fed PMBLDC motor drive

where v_{ao} , v_{bo} , v_{co} and v_{no} and are the voltages of the three phases (a, b, and c) and neutral point (n) with respect to the virtual midpoint of the dc link voltage shown as "o" in Fig. 2. The voltages v_{an} , v_{bn} and v_{cn} are the voltages of the three phases with respect to the neutral terminal of the motor (n), and *V*dc is the dc link voltage. The values 1 and 0 for *S*a1 or *S*a2 represent the "on" and "off" conditions of respective IGBTs of the VSI. The voltages for the other two phases of the VSI feeding the PMBLDC the PMBLDC motor,

i.e., v_{bo} , v_{co} , v_{bn} and v_{cn} and the switching pattern of the other IGBTs of the VSI (i.e., *S*b1, *S*b2, *S*c1, and *S*c2) are generated in a similar way.

(3) PMBLDC motor: The PMBLDCM is modeled in the form of a set of differential equations [2] given as

$$v_{an} = Ri_a + p\lambda_a + e_{an} \quad (17)$$

$$v_{bn} = Ri_b + p\lambda_b + e_{bn} \quad (18)$$

$$v_{cn} = Ri_c + p\lambda_c + e_{cn} \quad (19)$$

In these equations, p represents the differential operator (d/dt), i_a, i_b, and i_c are currents, λ_a, λ_b, and λ_c are flux linkages, and e_{an} , e_{bn} and e_{cn} are phase-to-neutral back EMFs of PMBLDCM, in respective phases; *R* is the resistance of motor windings/phase.

Moreover, the flux linkages can be represented as

$$\lambda_a = L_s i_a - M(i_b + i_c) \quad (20)$$

$$\lambda_b = L_s i_b - M(i_a + i_c) \quad (21)$$

$$\lambda_c = L_s i_c - M(i_b + i_a) \quad (22)$$

where *Ls* is the self-inductance/phase and *M* is the mutual inductance of PMBLDCM winding/phase.

The developed torque Te in the PMBLDCM is given as

$$T_e = (e_{an} i_a + e_{bn} i_b + e_{cn} i_c)/\omega_r \quad (23)$$

where ω_r is the motor speed in radians per se

Since PMBLDCM has no neutral connection

$$i_a + i_b + i_c = 0 \quad (24)$$

$$\lambda_a = (L_s + M)i_a,\ \lambda_b = (L_s + M)i_b,\ \lambda_c = (L_s + M)i_c \quad (26)$$

The current derivatives in generalized state-space form are given as

$$pi_x = (v_{xn} - i_x R - e_{xn})/(L_s + M) \quad (27)$$

where x represents phase a, b, or c.

The back EMF is a function of rotor position (θ) as

$$e_{xn} = K_b f_x(\theta)\omega_r \quad (28)$$

where x can be phase a, b, or c and accordingly $f_x(\theta)$ represents a function of rotor position with a maximum value ±1, identical to trapezoidal induced EMF, given as

$$f_a(\theta) = 1 \quad \text{for } 0 < \theta < 2\pi/3 \quad (29)$$

$$f_a(\theta) = 1\{(6/\pi)(\pi - \theta)\} - 1 \quad \text{for } 2\pi/3 < \theta < \pi \quad (30)$$

$$f_a(\theta) = -1 \quad \text{for } \pi < \theta < 5\pi/3 \quad (31)$$

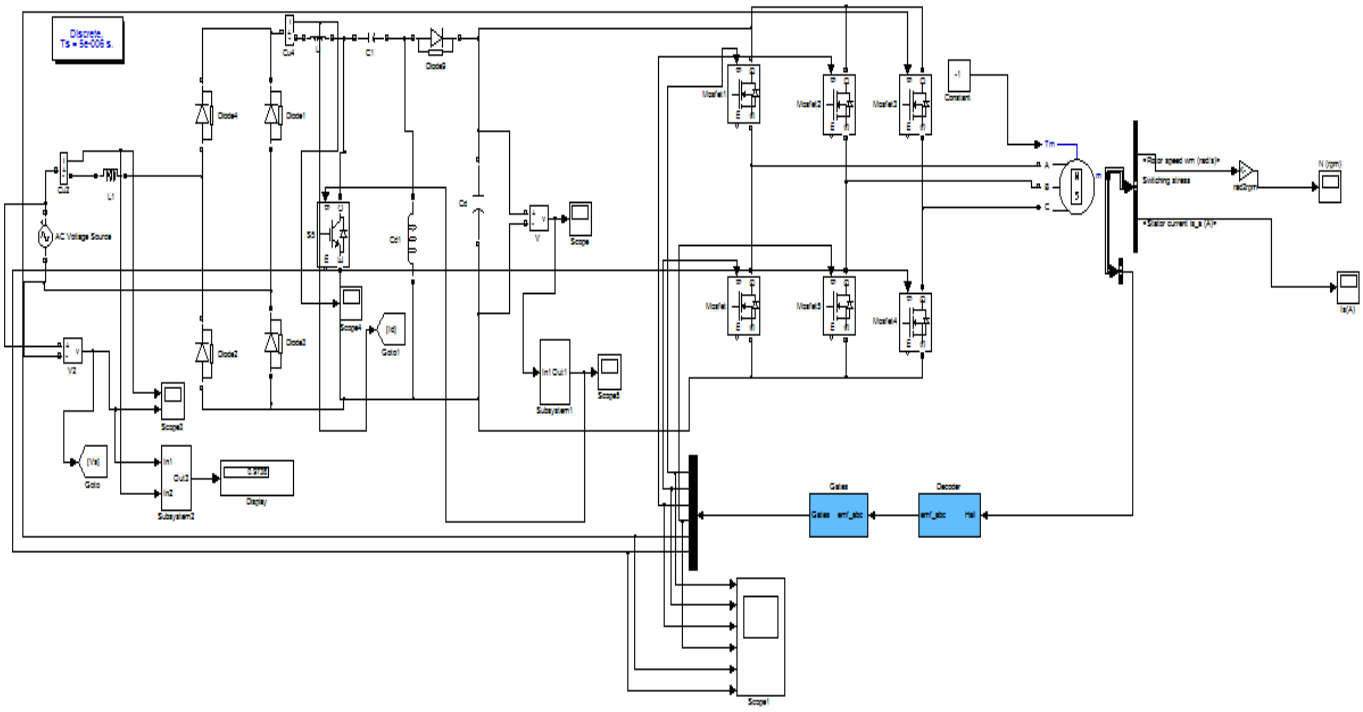
$$f_a(\theta) = \{(6/\pi)(\pi - \theta)\} + 1 \quad \text{for } 5\pi/3 < \theta < 2\pi \quad (32)$$

The functions $f_b(\theta)$ and $f_c(\theta)$ are similar to $f_a(\theta)$ with phase differences of 120◦ and 240◦, respectively.

Therefore, the electromagnetic torque is expressed as

$$T_e = K_b \{f_a(\theta)i_a + f_b + f_c(\theta)i_c\} \quad (33)$$

Fig.3 Simulation circuit of SEPIC PFC converter fed VSI based PMBLDCMD



deriva-

(34)

umber

of poles, T_l is the load torque in newton meters, J is the moment of inertia in kilogram square meters, and B is the friction coefficient in newton meter seconds per radian.

The derivative of rotor position is given as

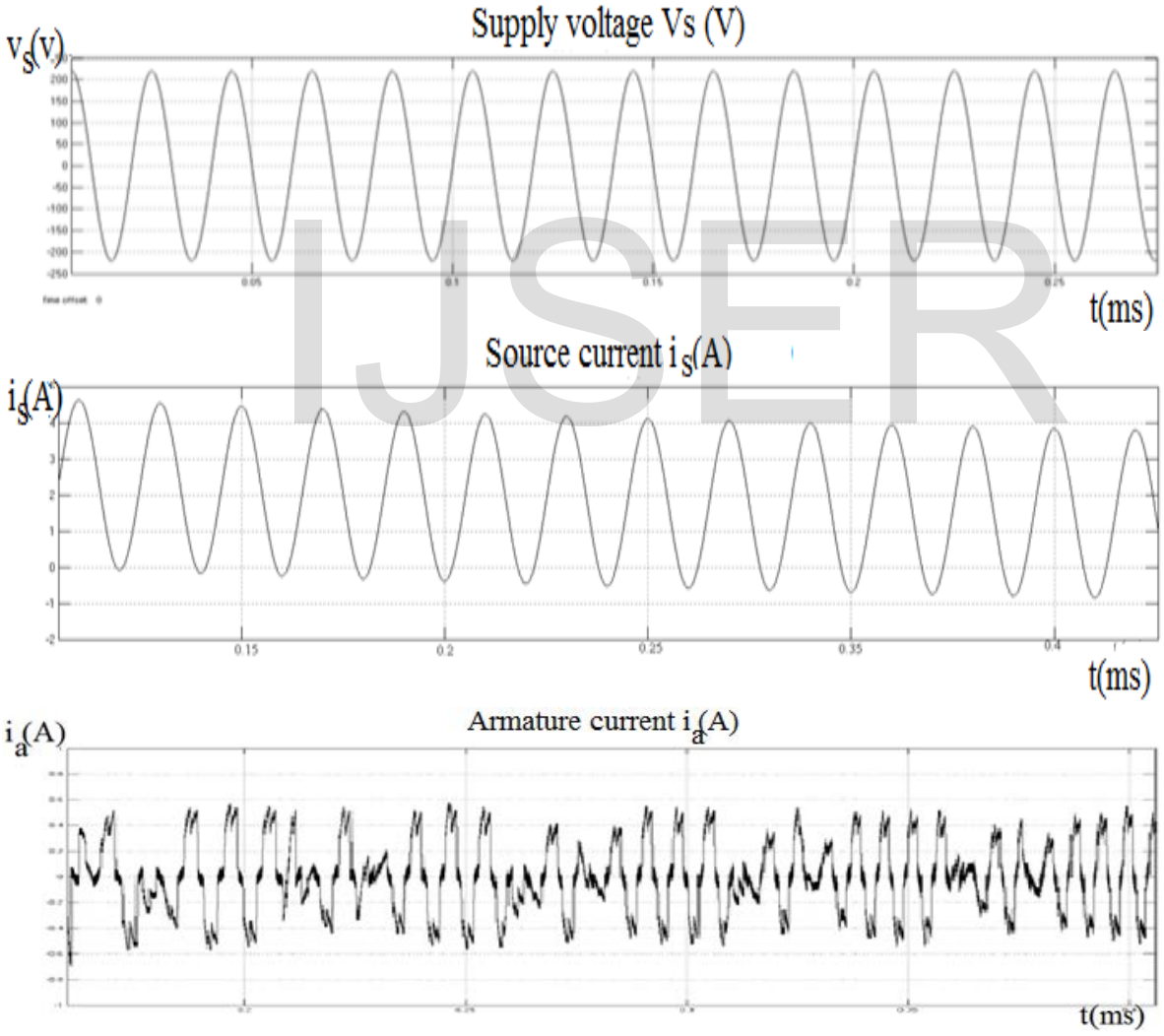
$$p\theta = \omega_r \quad (35)$$

The equations represent the dynamic model of the PMBLDC motor. A combination of these models represents the complete model of the drive [1].

V. PERFORMANCE EVALUATION OF PMBLDCMD

SIMULINK developed by Math Works is a commercial tool for modeling, simulating and analyzing multi domain dynamic systems.

The load is considered as a constant torque load equal to the rated torque (5.2 N m). A 10W rating PMBLDCM is used and its speed is controlled effectively by controlling the dc link voltage. For the performance evaluation of the proposed drive under input ac voltage variation, the dc link voltage is kept constant at 360 V which is equivalent to a 1000-r/min speed of the PMBLDCM. Fig.4 shows the obtained results of the performance of the PMBLDC drive under speed control at 220-V ac input voltage.



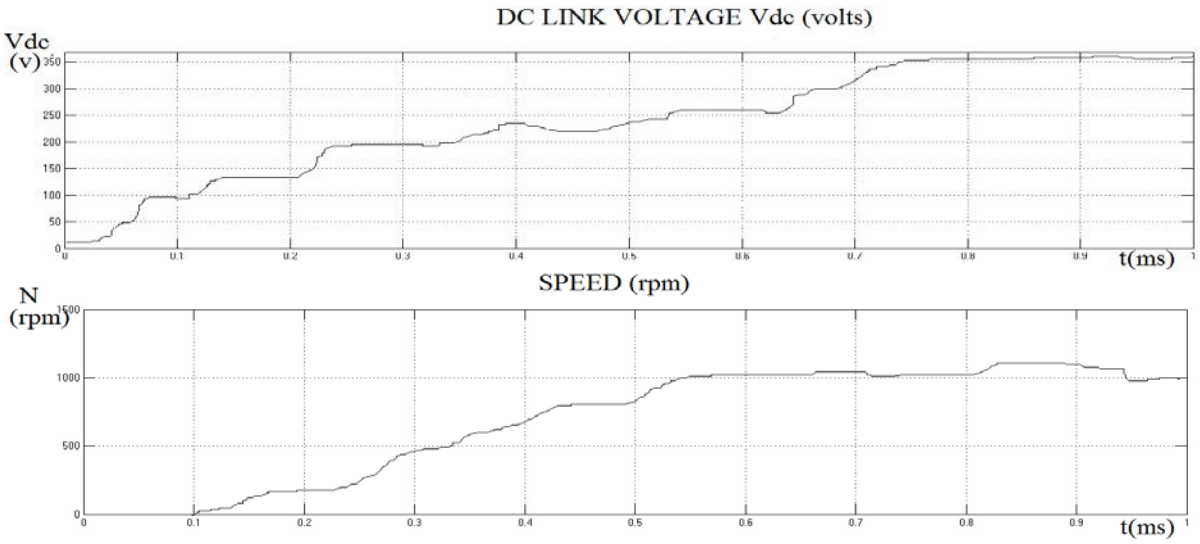


Fig.4 Performance of the PMBLDC drive under speed control at 220-v ac input voltage

The results obtained shows that the dc link voltage of the SEPIC PFC converter is more than that of the CUK converter [1], hence a wide range of speed is obtained by the SEPIC PFC converter fed PMBLDC motor. This also improves the power factor which is about 0.912.

VI.CONCLUSION

The speed control scheme for a PFC SEPIC converter based PMBLDC motor drive is simulated and implemented. It is found that the power factor is near unity with the use of the SEPIC converter. The speed of PMBLDCM has been found to be proportional to the dc link voltage and a smooth speed control is observed while controlling the dc link voltage. The introduction of a rate limiter in the reference dc link voltage effectively limits the motor current within the desired value. Due to the improved power factor, the SEPIC PFC converter fed PMBLDC motor can also be preferred in many applications.

REFERENCES

1. Sanjeev Singh and Bhim Singh , "*A Voltage-Controlled PFC Cuk Converter-Based PMBLDCM Drive for Air-Conditioners*", *IEEE Transactions On Industrial Applications*, vol. 48, no. 2, April 2012

2. I.Topaloglu, F.Krkmaz, H.Mamur, R.Gurbuz ,"*Closed-loop speed control of PM-BLDC motor fed by six step inverter and effects of inertia changes for desktop CNC machine*", *IEEE Transactions On Industrial Electronics*, vol. 19,no.1,May 2012

3.R.Antonio,D.Abud,"*Evaluation of boost, sepic and cuk topologies as power factor correction stage in electronic ballast applications*" , *IEEE Transactions On Industrial Electronics*, May 2008

of an LFR Based on a SEPIC Converter under Sliding mode control for HBLEDs applications", *IEEE Transactions On Industrial Electronics* ,May 2009

5. Ching-Jung Tseng, Chern-Lin Chen, "*A Novel Zero-Voltage-Transition PWM Cuk Power Factor Corrector*" , *IEEE Transactions On Industrial Electronics*, vol 46,no. 4, Aug 2004

6. Bhim Singh, Brij N. Singh, , Ambrish Chandra, "*A Review of Single-Phase Improved Power Quality AC–DC Converters*", , *IEEE Transactions On Industrial Electronics*, vol 50,no. 5, Oct 2003

R. Balahemalatha was born on 07th May 1990, in Dindigul, Tamilnadu. She received B.E. degree in Electrical and Electronics Engineering from Info Institute of Engineering, Coimbatore in the year 2012 from Anna University. She is currently pursuing her M.Tech. Degree in Power Electronics and Drives in the Department of Electrical and Electronics Engineering of B.S. Abdur Rahman University. Her area of interest includes Special Electrical Machines, Analysis of converters and Advanced power semiconductor devices.